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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/675,067	09/28/2000	Samson X. Huang	884.326US1	2844

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EXAMINER	
ALPHONSE, FRITZ	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 04/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/675,067	HUANG, SAMSON X.	
	Examiner	Art Unit	
	Fritz Alphonse	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2004* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *26-31* is/are allowed.

6)☒ Claim(s) *1-23 and 32-43* is/are rejected.

7)☒ Claim(s) *24 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

0.1 This office action is in response to amendment filed on 11/18/2004.

0.2 Claims 1-25 are pending. Claims 26-43 are added.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6, 9-15, 20, 32-34, 38-39 and 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishikawa (U. S. Pat. No. 5,805,604) in view of Shichiku (U.S. Pat. No. 6,317,817).

As to independent claims 1, 9, 15, 20, Nishikawa discloses a memory device 11 a with input and output data bus having a least significant bit and a plurality of non-least significant bits (see fig. 2, input and output to memory 11 a).

A first repair router is disclosed by "Rearranging Circuit" 12 with LSB input X0 and plural non-significant bit inputs X3 thru X1 and output data bus connected to memory 11 a. The Rearranging Circuit of Nishikawa routes any of the non-least significant bits to the least significant bit of the memory device, for example, see fig. 2 in which the most significant bit X3 has been routed to the position of the least significant bit (memory portion D).

Nishikawa does not explicitly discard the least significant bit (i.e., Nishikawa teaches that when there is a defect in a bit, other than the LSB, respective bits are rearranged so that the LSC is stored in the defect region). See col. 6, lines 10-15.

However, in the same field of endeavor, Shichiku discloses a memory device wherein the LSB is discarded (col. 8, lines 66-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the image operation processing apparatus, as disclosed by Shichiku. By doing so, it is possible to store data of the results of operation in continuous address of the memory, enabling efficient use of the memory areas. Since such a process can be realized by only one instruction, programming is facilitated (col. 11, lines 52-56).

Further, as to independent claim 15, Nishikawa discloses the bits can represent image data, which are inherently pixels; see col. 5, line 41.

Further, as to independent claim 20, Nishikawa discloses second repair router as "Rearranging Circuit" 13 wherein the first and second repair routers (Rearranging Circuits 12 and 13) route image bits as a function of defects in the memory 11 a. As to the routers include "internal routing circuitry to utilize any non-least significant bit of the memory device as a least significant bit", this is shown in fig. 2 wherein the defective memory location was section A (memory 11 a) and the least-significant bit "X0" has been routed to this location and the bit "X0", which previously corresponded to this location has been routed to the least-significant bit location D.

As to claims 2 and 33-34, a next-to-least significant bit of the memory device input data bus is disclosed as shown by the example in Table, error pattern 1100 wherein X1 next to LSB is utilized (see Nishikawa, tables 3-4).

As to claims 3, 12, 13 and 14, see discussion above directed to the second repair router disclosed by Nishikawa (Rearranging Circuit 13). As shown in fig. 2, the second repair router 13

reverses the routing performed by the first repair router, e.g., X3, X2, X1, X0 enters repair router 12 and X0, X2, X1, X3 is output by repair router 12 and the second repair router 13 has X0, X2, X1, X3 enter the second repair router followed by the reverse ordering of the routing performed by repair router 12, i.e., X3, X2, X1, X0 is output by repair router 13.

As to claims 4-5 and 10-11, (see Nishikawa fig. 9) with decoder 21 and ranges Am, Bm, and Cm where m is from 0-7 see col. 11, lines 12-60.

As to claim 6, Nishikawa teaches that the bits can represent image data, which are inherently pixels (col. 5, line 41).

Method claims 32 and 38-39, 41-43 method claims 32 and 38-39 correspond to apparatus claims 1 and 20. Therefore, they are analyzed as previously discussed in claims 1 and 20 above.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7-8 and 16-19, 21-23, 35-37, 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishikawa and Shichiku as applied to claims 1 and 15 and 20 above, and further in view of Kondo (U.S. Pat. No. 5,153,574).

As to claims 7-8, 35-37, Nishikawa is directed to an apparatus and method for handling memory defects by routing non-least significant image bits to least-significant image bit locations in memory.

Nishikawa does not teach a second and third memory device along with a second and third pair of repair routers. Nishikawa is also silent as to the type of display in which his images are displayed, i.e., Nishikawa does not teach a silicon light modulator.

Kondo teaches an interface for a thin display which can include a liquid crystal display (col. 1, lines 9-11) which is the same as the silicon light modulator described by Applicant on page 1, lines 9-10 of the specification. Kondo includes three memory devices (RAMs 211, 212, and 213) for storing red, green and blue pixel data, see col. 3, lines 13-15.

It would have been obvious to use the memory defect routing of Nishikawa in a LCD display system with three memories for color display. This would have been obvious as suggested by Nishikawa wherein Nishikawa's device is used for image data, "A rearranging circuit 12 has a function to rearrange respective bits representing image data..." col. 5, and lines 40-41 of Nishikawa.

Further, since Nishikawa is directed at providing a method and apparatus to mitigate memory defects without requiring the extra overhead of spare memory, it would have been obvious to include the rearranging circuits (i.e., rerouting circuitry) to the device of Kondo so as not to require extra memory and to require a change in the size of the memory. As combined, the system of Kondo and Nishikawa would simply add the input rearranging circuits 12 (first repair router) of Nishikawa to each of the inputs of memories 211, 212 and 213 of Kondo and add the output rearranging circuits 13 (second repair router) of Nishikawa on the outputs of memories 211, 212, and 213 of Kondo.

As directed to claims 7, 17, 18 and 23, the combined system of Kondo and Nishikawa includes a three separate color memories, each with a pair of repair router circuitry.

As to claims 16, 21and 40, the system of Kondo includes an interface for a liquid crystal display which is the same as the claimed silicon light modulator and as to claim 21, the use of a reflective electrode is well known in the art and would be obvious to use in a liquid crystal device without a back-light, i.e., these type of LCD displays are typical in watches or front lit displays, examiner will provide references if desired.

As to claims 19 and 22, Nishikawa shows groupings as shown in the control of fig. 8, see also fig. 11 wherein the bits are grouped into 4 groups of 4 bits.

Allowable Subject Matter

5. Claims 24 –25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claim 26 is allowable because none of the cited references teaches "a first repairable memory coupled to the green display device to drive the green display device; a second repairable memory coupled to the blue display device to drive the blue display device; a third repairable memory coupled to the red display device to drive the red display device ". In addition, claims 27-31 are allowable by virtue of dependency.

Response to Arguments

7. Applicant's arguments filed 11/18/04 have been fully considered but they are not persuasive.

On page 11 of Remarks, applicant asserts, "Shichiku issued on 13 November 2001, which is after the filing data of the present application. The applicant does not admit that Schichiku is prior art."

8. The examiner respectfully disagrees with applicant's statement. First, Schichiku (U.S. Pat. No. 6,317,817) issued on 13 November 2001 has been filed on May 14, 1998 about two years before the filing data of the present application (which filing date is September 28, 2000). Second, Schichiku assignee is different. Schichiku is a valid prior art. Therefore, the rejection is proper.

On page 12-15 of Remarks, applicant argues that the Office Action does not provide suggestions or motivations to combine references.

The motivation to combine references is clearly stated in the Office Action. The examiner respectively refers the applicant back to the rejection above because all the limitations of the claims are fully addressed in the Office Action.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

Or faxed to: (703) 872-9306 for all formal communications.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fritz Alphonse, whose telephone number is (571) 272-3813. The examiner can normally be reached on M-F, 8:30-6:00, Alt. Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fritz Alphonse

Art Unit 2133

April 13, 2005

GUY LAMARRE
PRIMARY EXAMINER